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Su et al.

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(54) **METHODS FOR INTRODUCING CARBON TO A SEMICONDUCTOR STRUCTURE**

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(51) **Int. Cl.**

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H01L 21/225	(2006.01)
H01L 21/265	(2006.01)
H01L 29/66	(2006.01)
H01L 29/78	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/225*** (2013.01); ***H01L 21/26586*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/66606*** (2013.01); ***H01L 29/7833*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/76829; H01L 29/7831; H01L 21/76825; G23C 16/26

USPC 438/795, 530; 257/E21.247, E21.249

See application file for complete search history.

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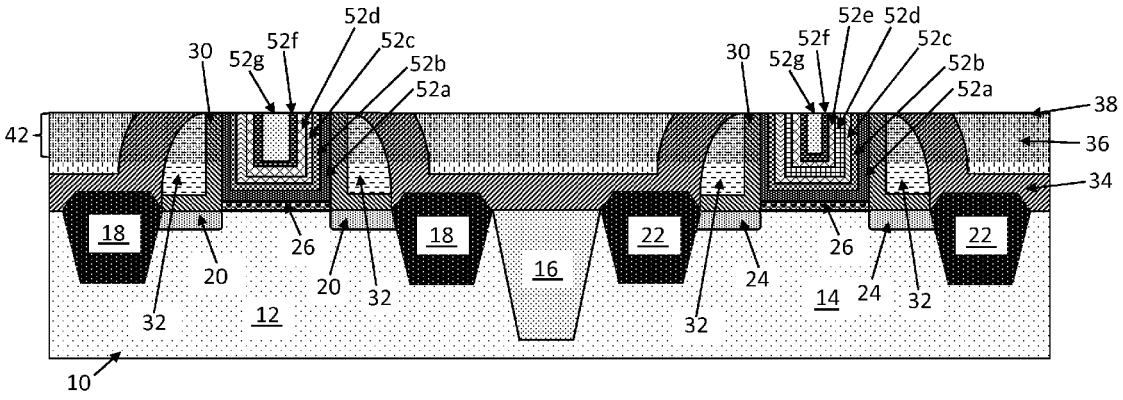
(57) **ABSTRACT**

An embodiment is a method comprising diffusing carbon through a surface of a substrate, implanting carbon through the surface of the substrate, and annealing the substrate after the diffusing the carbon and implanting the carbon through the surface of the substrate. The substrate comprises a first gate, a gate spacer, an etch stop layer, and an inter-layer dielectric. The first gate is over a semiconductor substrate. The gate spacer is along a sidewall of the first gate. The etch stop layer is on a surface of the gate spacer and over a surface of the semiconductor substrate. The inter-layer dielectric is over the etch stop layer. The surface of the substrate comprises a surface of the inter-layer dielectric.

20 Claims, 5 Drawing Sheets



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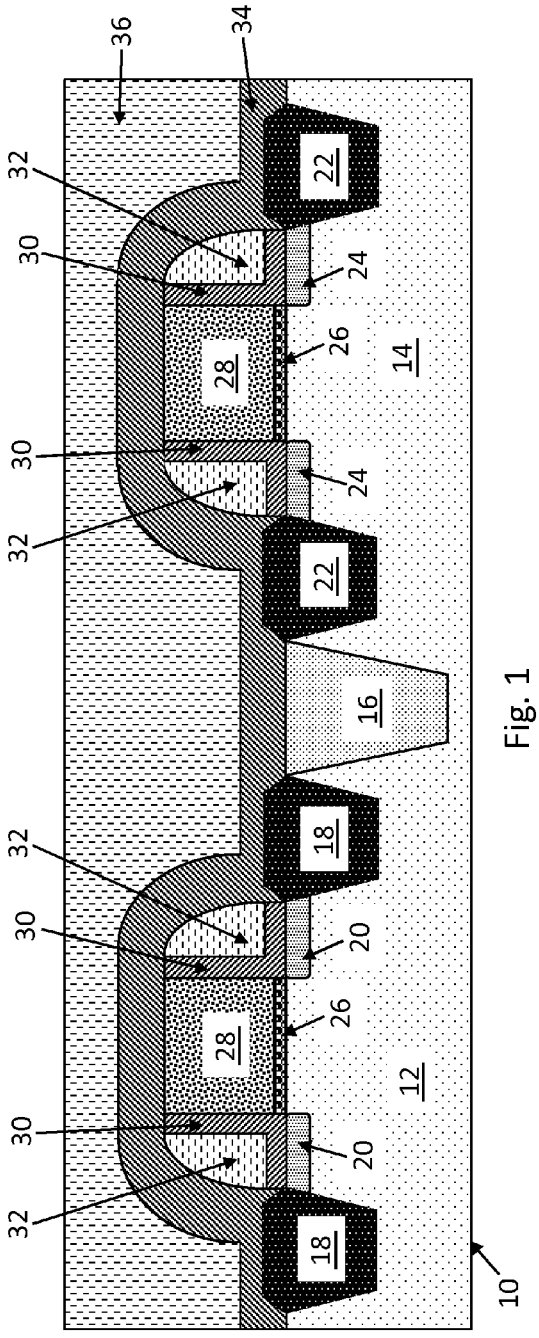
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Fig. 1

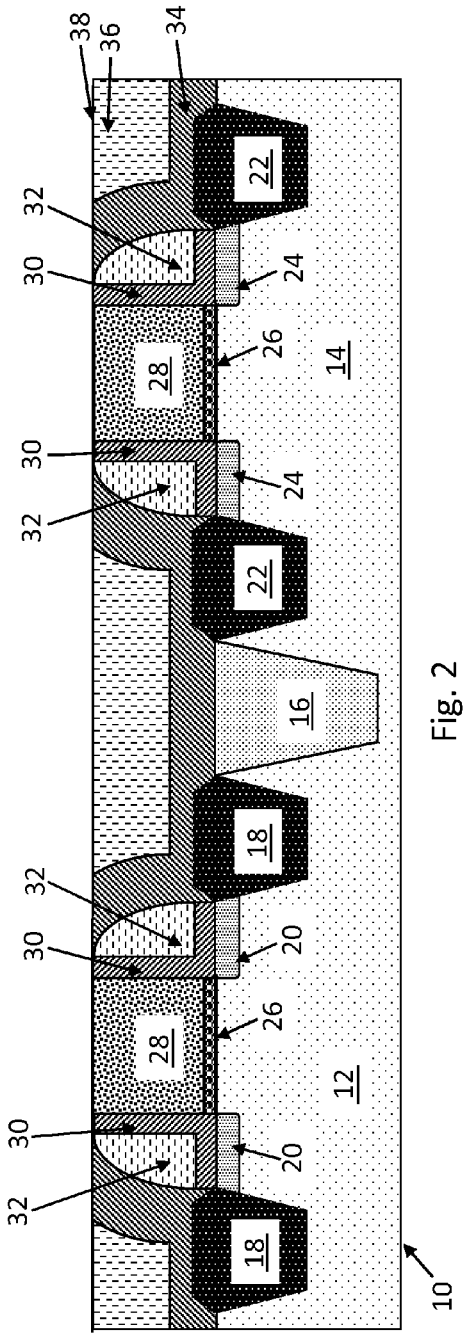
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Fig. 2

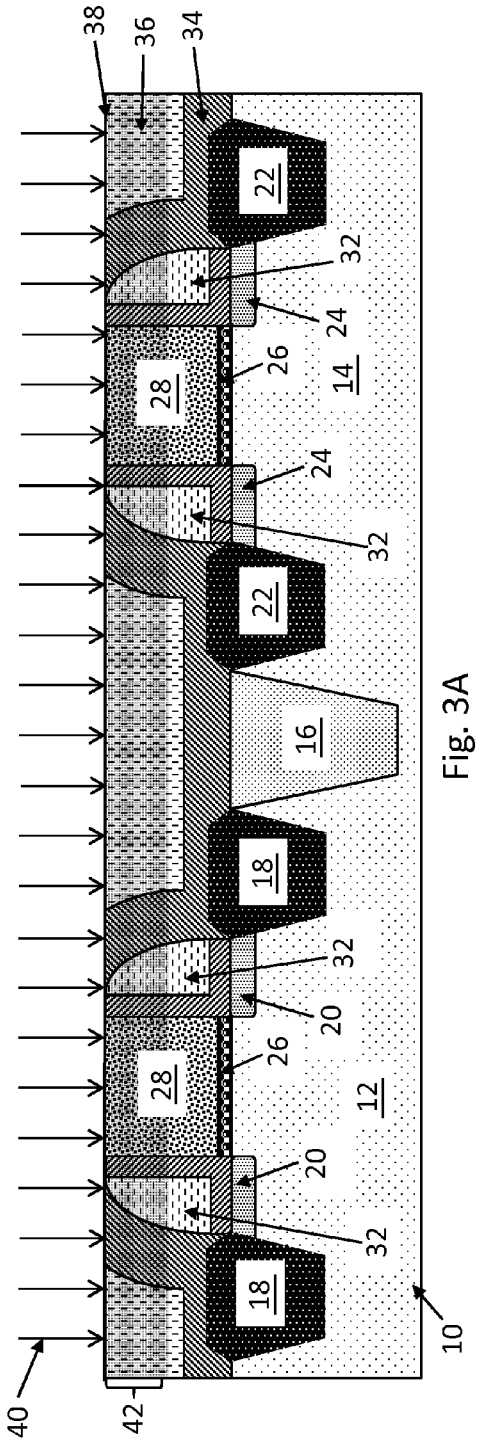
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Fig. 3A

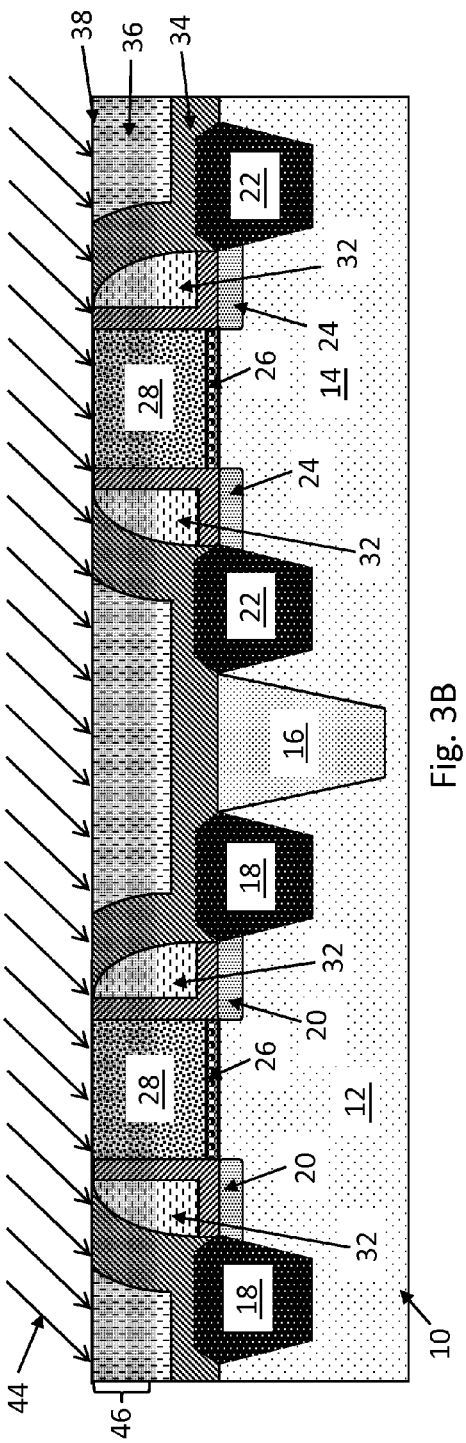
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Fig. 3B

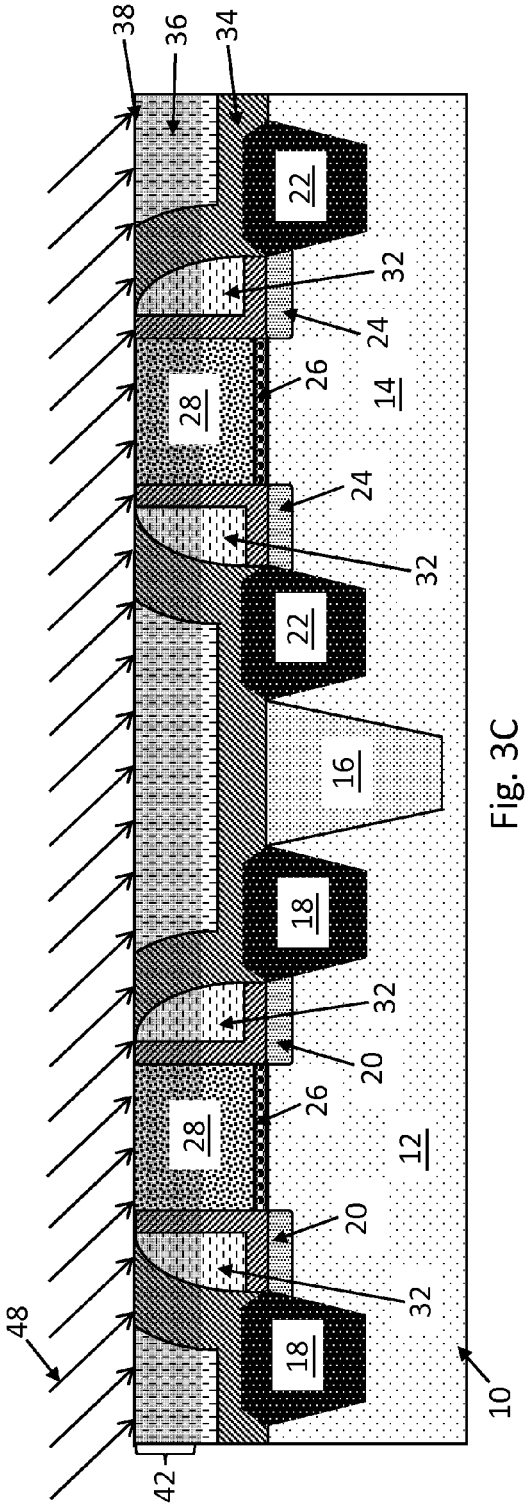
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Fig. 3C

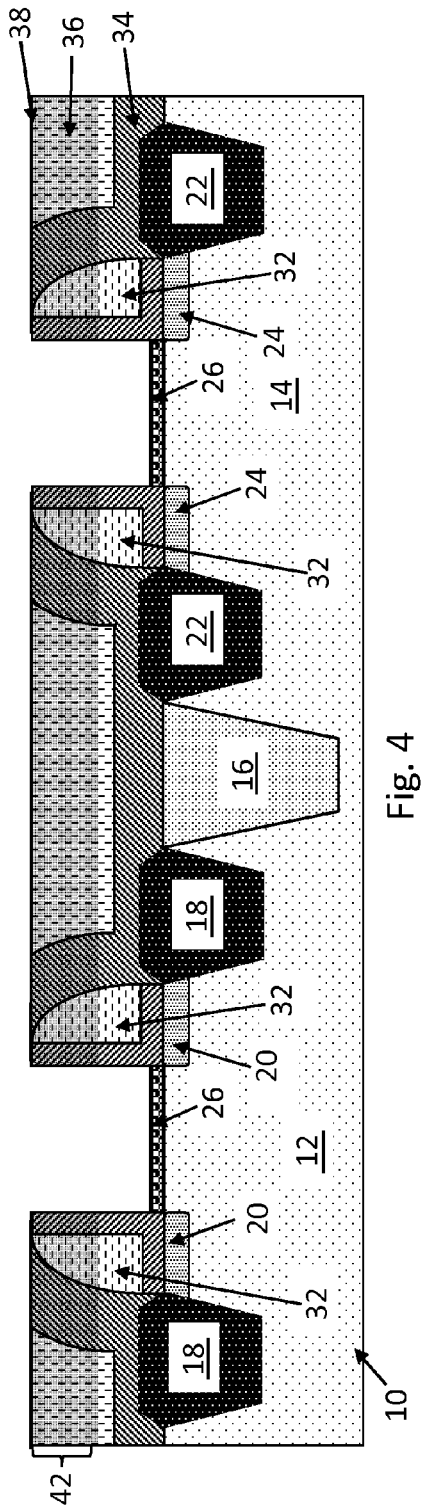
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Fig. 4

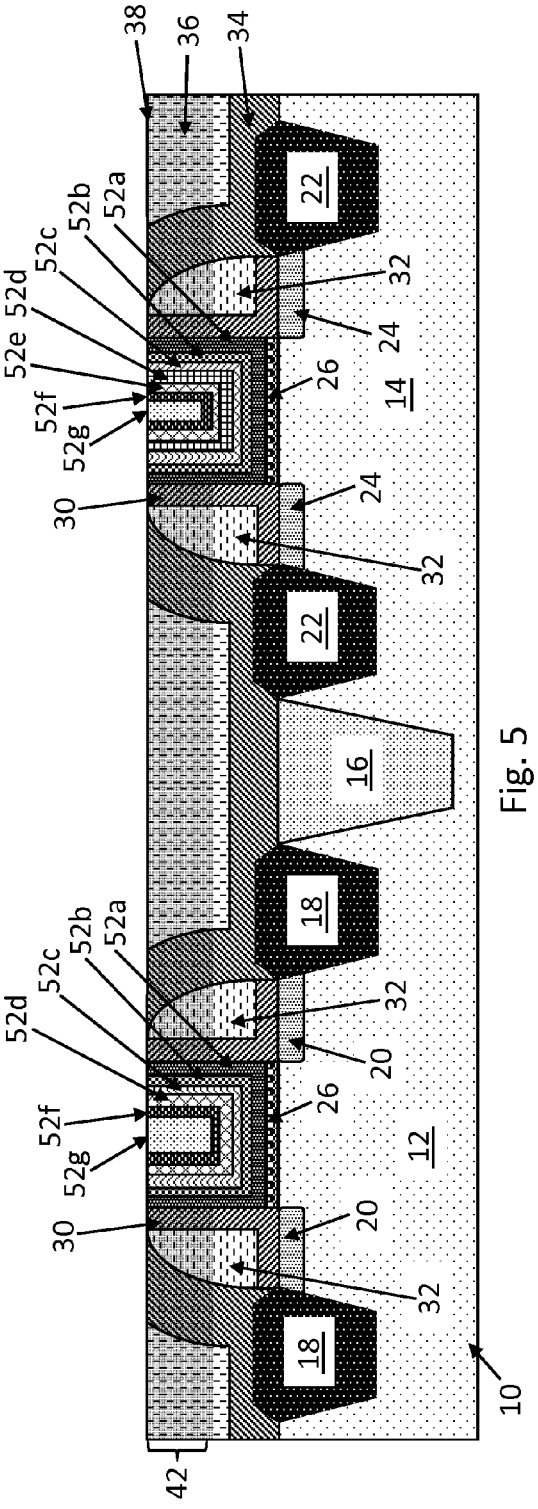
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Fig. 5

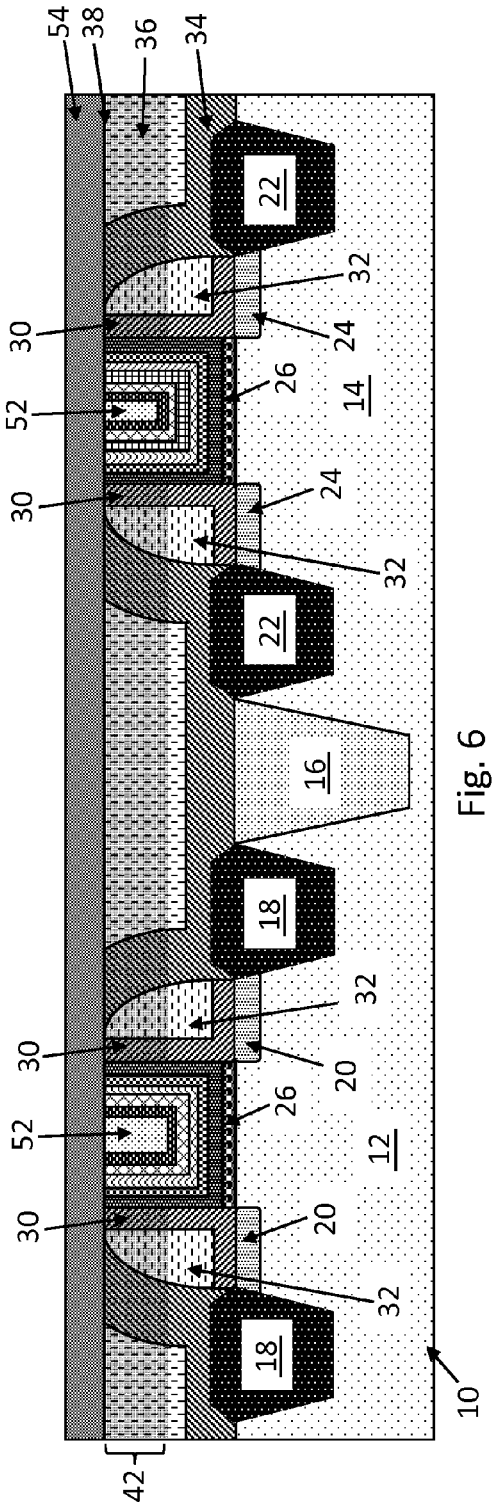
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Fig. 6

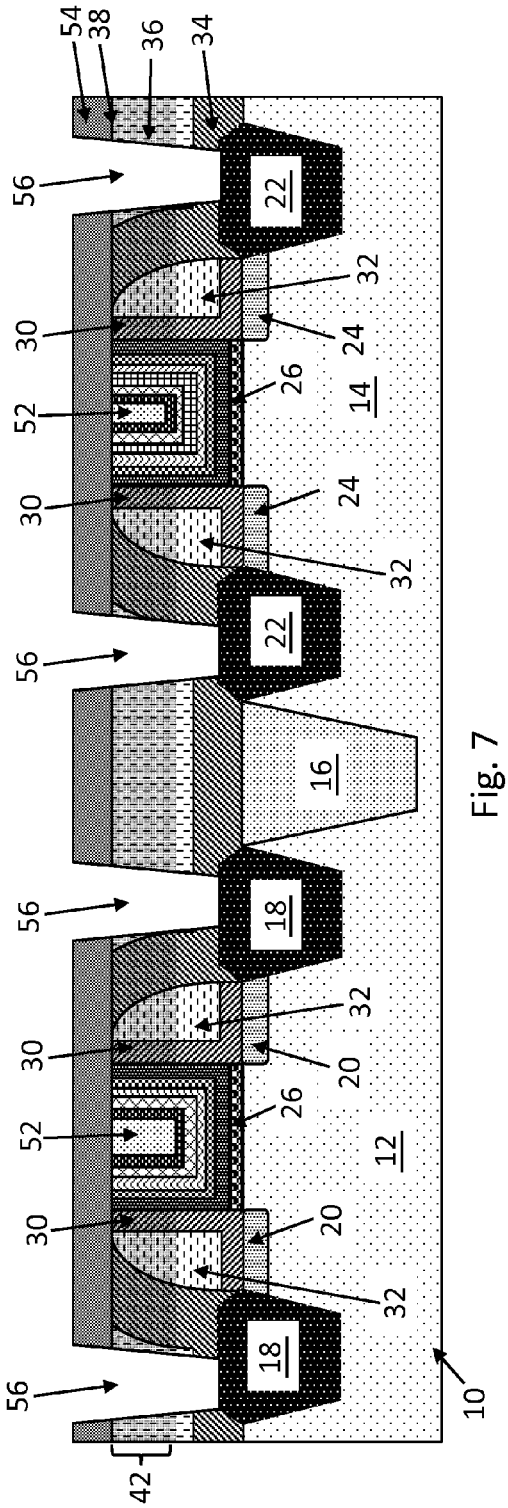
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Fig. 7

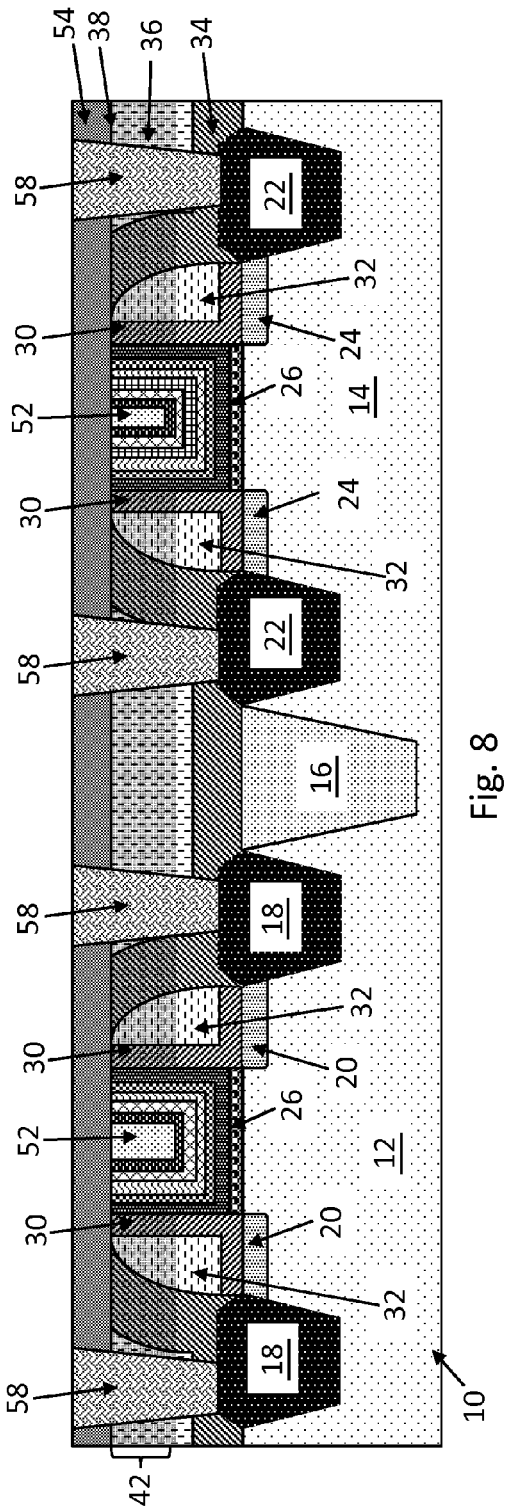
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Fig. 8

METHODS FOR INTRODUCING CARBON TO A SEMICONDUCTOR STRUCTURE

BACKGROUND

Since the development of the integrated circuit (IC), the semiconductor industry has sought to continue to improve the performance or size of the IC. Many of these improvements have focused on smaller feature sizes so that the speed of the IC can be increased. By decreasing the feature sizes, the density of devices (e.g., transistors, diodes, resistors, capacitors, etc.) on the IC has increased. By increasing the density, distances between devices generally decreases, which allows for a smaller resistance and capacitance between devices. Thus, a resistance-capacitance (RC) time constant can be decreased.

With the decrease in distances between devices generally comes more difficulty in ensuring proper alignment of features, such as contacts, in overlying layers with features in an underlying substrate, such as a source or drain. Tolerances can become very small in smaller technology nodes, and a small amount of misalignment of an overlying layer can cause overlay problems that can render devices faulty.

Further, features in devices that are intended to prevent faults in the case of misalignment can become thinner and weaker in smaller technology nodes. These thinner layers may not be able to withstand an etchant that is not selective to the layers. Even further, these features can be exposed to multiple etchants from various sides, particularly in the developing gate-last processes that are now being developed. The attacks on these features by the etchants can cause a subsequent unintended short circuit between conductive features, which can render devices useless.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1**, **2**, **3**A, **3**B, **3**C, and **4** through **8** are methods of forming a CMOS structure according to embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosed subject matter, and do not limit the scope of the different embodiments.

Embodiments will be described with respect to a specific context, namely a method to form a CMOS structure and the CMOS structure. The CMOS structure can include planar or fin field effect transistors. Further, a gate-last process is described herein, and other embodiments contemplate a gate-first process. The disclosed methods and structures are described in the context of a 20 nm technology node or smaller, and other embodiments contemplate different technology nodes. The methods disclosed herein are described in an example order. Other embodiments contemplate methods performed in any logical order. Like reference numerals in the figures refer to like components.

FIG. **1** illustrates an intermediate structure during processing according to an embodiment. The structure includes a substrate **10** having an n-type device region **12** ("n-region") and a p-type device region **14** ("p-region") separated by an isolation region **16**. The substrate **10** is, for example, a bulk silicon substrate, a semiconductor on insulator (SOI) substrate, or another semiconductor substrate. The n-region **12** can be for a NMOS, n-type finFET, core NMOS or n-type finFET, or the like, and can include a p-type doped well. The p-region **14** can be for a PMOS, p-type finFET, core PMOS or p-type finFET, or the like, and can include an n-type doped well. The isolation region **16** can be a shallow trench isolation (STI), a field oxide, or the like.

Respective gate dielectrics **26** and dummy gates **28** are formed over the regions **12** and **14** of the substrate **10**. To form these components, a dielectric layer is deposited over the substrate **10**. The dielectric layer can be silicon oxide, silicon oxynitride, the like, or a combination thereof, formed by chemical vapor deposition (CVD), plasma-enhanced CVD (PECVD), the like, or a combination thereof. A dummy layer is deposited over the dielectric layer. The dummy layer in this embodiment is polysilicon, although other materials can be used, and can be deposited using CVD, atomic layer deposition (ALD), the like, or a combination thereof. A photoresist can then be deposited over the dummy layer, such as by spin-on deposition, and patterned by exposure to light. An etch can then remove portions of the dummy layer and dielectric layer that are not covered by the photoresist, thereby patterning the dummy gates **28** and the gate dielectrics **26**. In an example embodiment, a top surface of the dummy gate **28** is a distance from a top surface of the substrate **10** in a direction normal to the top surface of the substrate, and the distance is approximately 450 Angstroms (Å). Other acceptable techniques for forming the gate dielectrics **26** and dummy gates **28** may also be used.

After the gate dielectrics **26** and dummy gates **28** are formed, n-type low-doped extension regions **20** in the n-region **12** and p-type low-doped extension regions **24** in the p-region **14** are formed. A first masking layer, such as a photoresist, can be patterned over the p-region **14**, and n-type dopants, such as phosphorus, arsenic, the like, or a combination thereof, can be implanted into the n-region **12**. The first masking layer is then removed. A second masking layer, such as a photoresist, can be patterned over the n-region **12**, and p-type dopants, such as boron, the like, or a combination thereof, can be implanted into the p-region **14**. Other acceptable techniques can be used for forming the low-doped extension regions **20** and **24**.

Spacer liners **30** and spacers **32** are formed on sidewalls of the dummy gates **28** and gate dielectrics **26**. A thin dielectric layer can be conformally deposited over the substrate **10** and dummy gates **28** and along sidewalls of the dummy gates **28** and gate dielectrics **26**. The thin dielectric layer can be silicon nitride, silicon oxide, silicon oxynitride, the like or a combination thereof, formed by a CVD, the like, or a combination thereof. A spacer dielectric layer can be conformally deposited over the thin dielectric layer. The spacer dielectric layer can be silicon nitride, silicon oxide, silicon oxynitride, the like or a combination thereof, formed by a CVD, the like, or a combination thereof. An anisotropic etch can then pattern the dielectric layers into the spacer liners **30** and spacers **32** along the sidewalls. Other acceptable techniques can be used for forming the spacers **32** and spacer liners **30**.

Source/drain regions **18** and **22** are formed in the n-region **12** and the p-region **14** of the substrate **10**, respectively. In an embodiment, trenches are etched in the substrate **10** along edges of the spacers **32** and spacer liners **30** opposite the

dummy gate **28**. A first semiconductor material is epitaxially grown in the trenches in the n-region **12**, and a second semiconductor material is epitaxially grown in the trenches in the p-region **14**. These epitaxial semiconductor materials can be grown to a height above a top surface of the substrate **10** and may have facets between respective top surfaces of the epitaxial semiconductor materials and the top surface of the substrate **10**. Example materials for the first semiconductor material in the n-region **12** include silicon phosphorus, silicon carbide, the like, or a combination thereof, formed by, for example, selective epitaxial growth (SEG) or the like. Example materials for the second semiconductor material in the p-region **14** include silicon germanium, the like, or a combination thereof, formed by, for example, SEG or the like. The epitaxial material materials in the n-region **12** and the p-region **14** may be doped with n-type dopants and p-type dopants, respectively, in situ during growth or after growth by an implant. Various masks may be used during etching, epitaxial growth, and/or doping. In another embodiment, the substrate **10** in the n-region **12** and the p-region **14** can be doped by an implant with n-type dopants and p-type dopants, respectively, to form the source/drain regions **18** and **22**, respectively, without epitaxial materials. Other appropriate techniques can be used for forming the source/drain regions **18** and **22**.

An etch stop layer (ESL) **34** is formed over the substrate **10**, dummy gates **28**, spacers **32**, spacer liners **30**, and source/drain regions **18** and **22**. The ESL **34** is conformally deposited over components on the substrate **10**. The ESL **34**, in an embodiment, is silicon nitride, and may also be other like materials or a combination thereof. The ESL can be formed by CVD, the like, or a combination thereof.

An inter-layer dielectric (ILD) **36** is formed over the ESL **34**. The ILD **36**, in an embodiment, is silicon oxide, and may also be other like materials or a combination thereof. The ILD **36** can be formed by CVD, a high density plasma (HDP), the like, or a combination thereof.

In FIG. **2**, the ILD **36** and ESL **34** are planarized to a top surface of the dummy gate **28** forming a planarized surface **38**. In an embodiment, the ILD **36** and ESL **34** are planarized by using a chemical mechanical polish (CMP) to remove portions of the ILD **36** and ESL **34** to the planarized surface **38**. In other embodiments, other planarization techniques may be used, such as including etching.

The planarized surface **38** is exposed to a carbon plasma. Example parameters of the carbon plasma include the following: pressure between about 1 mT and about 20 mT; power between about 100 W and about 300 W; frequency between about 2 MHz and about 13.6 MHz; time of exposure between about 30 seconds to about 300 seconds; and a pulse DC duty ratio between about 20% and about 80%. The carbon in the plasma reacts with the planarized surface **38**. Carbon can diffuse from the planarized surface **38** to a depth below the planarized surface **38**, such as in the ILD **36**, the ESL **34**, the spacers **32**, and/or spacer liners **30**. As with a diffusion, a concentration of carbon can decrease from the planarized surface **38** to the depth. In an embodiment, a carbon concentration at the planarized surface **38** is between approximately 1×10^{10} cm^{-3} and approximately 1×10^{17} cm^{-3}.

In FIG. **3**A, carbon is implanted **40** to a depth below the planarized surface **38**. The carbon is implanted **40** into, for example, the ILD **36**, the ESL **34**, the spacers **32**, and/or spacer liners **30**. The implantation **40** is at an angle that is normal to the planarized surface **38**. The carbon can be implanted at a depth between approximately 150 Å and approximately 200 Å below the planarized surface **38**. The implant can be at a depth between approximately one-third to one-half the distance of the top surface of the dummy gates **28** (e.g., the planarized surface **38**) to the top surface of the substrate **10**. The implant can use an energy between approximately 2 keV and approximately 10 keV. A concentration of the carbon at the depth below the planarized surface can be between approximately $1\times10^{14}/cm^3$ and approximately $1\times10^{15}/cm^3$. As with an implantation, a concentration of the implanted species can have a gradient as a function of depth, such as increasing to a depth where the concentration is greatest and then decreasing towards further depths.

After the plasma and implantation **40**, the structure can have a substantially uniform concentration of carbon from the planarized surface **38** to the depth, although in other embodiments, the concentration varies over this distance. The decrease in carbon concentration due to the diffusion can be offset by an increase in carbon concentration due to the implantation as the distance from the planarized surface **38** increases. In other embodiments, the concentrations from the different steps are not offset, and the total concentration in the structure can vary as a function of distance from the planarized surface **38**.

After the plasma and implantation **40**, the structure is annealed resulting in a carbon-containing region **42**. The anneal, such as a rapid thermal anneal, can be at a temperature between approximately 700° C. and approximately 1,300° C., such as approximately 1,000° C., for a duration between approximately 0.001 second and approximately 30 minutes. The anneal reacts the carbon with the materials of the ILD **36**, the ESL **34**, spacers **32**, and spacer liners **30** in the carbon-containing region **42**. In an embodiment where the ILD **36** is silicon oxide and each of the ESL **34**, spacers **32**, and spacer liners **30** is silicon nitride, the anneal results in silicon oxycarbide and silicon carbon nitride, respectively, in the carbon-containing region **42**. It should be noted that portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** below the carbon-containing region **42** can have a lower concentration of carbon, such as substantially negligible, than portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** in the carbon-containing region **42**. Hence, these lower portions can remain silicon oxide and silicon nitride, respectively, after the anneal.

FIGS. **3**B and **3**C are another example to implant carbon. In FIG. **3**B, carbon is implanted **44** to a depth below the planarized surface **38** at a first tilt angle to form a first carbon implant region **46**. The carbon is implanted **44** into, for example, the ILD **36**, the ESL **34**, the spacers **32**, and/or spacer liners **30**. The first tilt angle, in this example, is in a plane that is perpendicular to sidewalls of the dummy gates **28** and perpendicular to the planarized surface **38**. The first tilt angle is in the plane and is between approximately 0° and approximately 90°, such as 45°, from an axis normal to the planarized surface **38** measured in a clockwise manner. The selection of a tilt angle can depend upon the pitch between the dummy gates **28** and the orientation of the dummy gates **28**. The carbon can be implanted at a depth between approximately 150 Å and approximately 200 Å below the planarized surface **38**. The implant can be at a depth between approximately one-third to one-half the distance of the top surface of the dummy gates **28** (e.g., the planarized surface **38**) to the top surface of the substrate **10**. The implant can use an energy between approximately 2 keV and approximately 10 keV.

In FIG. **3**C, carbon is implanted **48** to a depth below the planarized surface **38** at a second tilt angle. The carbon is implanted **48** into, for example, the ILD **36**, the ESL **34**, the spacers **32**, and/or spacer liners **30**. The second tilt angle, in this example, is complementary to the first tilt angle and is in the plane that is perpendicular to sidewalls of the dummy

gates **28** and perpendicular to the planarized surface **38**. The second tilt angle is in the plane and is between approximately 0° and approximately 360°, such as 315°, from an axis normal to the planarized surface **38** measured in a clockwise manner (e.g., 45° from the axis measured in a counter-clockwise manner). The carbon can be implanted at a depth between approximately 150 Å and approximately 200 Å below the planarized surface **38**. The implant can be at a depth between approximately one-third to one-half the distance of the top surface of the dummy gates **28** (e.g., the planarized surface **38**) to the top surface of the substrate **10**. The implant can use an energy between approximately 2 keV and approximately 10 keV. A concentration of the carbon at the depth below the planarized surface can be between approximately 1×10^{14}/cm^3 and approximately 1×10^{15}/cm^3. As with an implantation, a concentration of the implanted species can have a gradient as a function of depth.

After the plasma and implantations **44** and **48**, the structure can have a substantially uniform concentration of carbon from the planarized surface **38** to the depth, although in other embodiments, the concentration varies over this distance. The decrease in carbon concentration due to the diffusion can be offset by an increase in carbon concentration due to the implantation as the distance from the planarized surface **38** increases. In other embodiments, the concentrations from the different steps are not offset, and the total concentration in the structure can vary as a function of distance from the planarized surface **38**.

After the plasma and implantations **44** and **48**, the structure is annealed resulting in a carbon-containing region **42**. The anneal, such as a rapid thermal anneal, can be at a temperature between approximately 700° C. and approximately 1,300° C., such as approximately 1,000° C., for a duration between approximately 0.1 second and approximately 30 minutes. The anneal reacts the carbon with the materials of the ILD **36**, the ESL **34**, spacers **32**, and spacer liners **30** in the carbon-containing region **42**. In an embodiment where the ILD **36** is silicon oxide and each the ESL **34**, spacers **32**, and spacer liners **30** is silicon nitride, the anneal results in silicon oxycarbide and silicon carbon nitride, respectively, in the carbon-containing region **42**. It should be noted that portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** below the carbon-containing region **42** can have a lower concentration of carbon, such as substantially negligible, than portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** in the carbon-containing region **42**. Hence, these lower portions can remain silicon oxide and silicon nitride, respectively, after the anneal.

The introduction of carbon, such as by the plasma exposure and/or by implantation, to portions of the ESL **34**, spacers **32**, and spacer liners **30** and subsequent anneal can increase the density of each component. Thus, portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** below the carbon-containing region **42** can have a lower density than portions of the ILD **36**, ESL **34**, spacers **32**, and spacer liners **30** in the carbon-containing region **42**.

In FIG. **4**, the dummy gates **28** are removed. The dummy gates **28** may be removed by an etch that is selective to the material of the dummy gates **28**. It should be noted that different etchants may be used if carbon is also implanted into the dummy gates **28** such that portions of the dummy gates **28** contain carbon and others do not. For example, if the dummy gates **28** comprise polysilicon, top portions of the dummy gates **28** in the carbon-containing region **42** may be silicon carbide, and bottom portions are silicon. A first etch using, for example, CF_4 may remove the top portions, and a second etch using, for example, NF_3, SF_6, Cl_2, HBr, the like, or a combination thereof may remove the bottom portions.

In FIG. **5**, gate structures **52** are formed in the regions where the dummy gates **28** were removed. Various sub-layers **52***a*-**52***g* can be included in the gate structures **52**. Some of the sub-layers can each be a high-k dielectric layer, such as $HfSiO_4$, HfSiON, HfSiN, ZrSiO4, ZrSiON, ZrSiN, ZrO_2, HfO_2, La_2O_3, or the like. Other sub-layers over the high-k dielectric layers can be metal layers, such as tungsten, titanium nitride, or the like. The sub-layers **52***a*-**52***g* are subsequently conformally deposited over the ILD **36** and in the region where the dummy gates **28** were removed, for example, using CVD, ALD, thermal deposition, or the like. A planarization, such as by CMP, removes excess materials of the layers over the planarized surface **38** to form the gate structures **52**. In embodiments, some of sub-layers **52***a*-**52***g* are not formed in both gate structures **52**. For example, sub-layer **52***e* is not in the gate structure **52** over the n-region **12**. This can be achieved by removing the sub-layer **52***e* using an etch, for example, while the gate structure **52** over the p-region **14** is masked. By having different sub-layers, different work functions of the devices may be achieved.

In FIG. **6**, a CESL **54** is formed over the planarized surface **38**. The CESL **54** can be a silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, the like, or a combination thereof, formed by a CVD, ALD, thermal deposition, the like, or a combination thereof. In FIG. **7**, contact openings **56** are etched through the CESL **54**, ILD **36**, and CESL **34** to respective source/drain regions **18** and **22**. A photoresist can be patterned over the CESL **54** and one or more etch steps can form the contact openings **56**. In FIG. **8**, contacts **58** are formed to respective source/drain regions **18** and **22** in the contact openings **56**. A conductive material, such as a metal, can be deposited in the contact openings **56** and excess of the conductive material can be removed, such as by a CMP, to form the contacts **58**. In other embodiments, another ILD can be formed over the CESL **54**, and contact openings can be etched through the ILD, the CESL **54**, ILD **36**, and CESL **34** using respective etch steps. Contacts can be formed in the contact openings.

Embodiments may achieve a more robust spacer and etch stop layer to self-align contacts. The carbon plasma exposure and implant with subsequent anneal can make the spacers and etch stop layer denser, and the spacers and etch stop layer can thus have a slower etch rate than without carbon. The spacers and etch stop layer can be more robust against the etchant removing the dummy gates and the etchant etching the ILD to form a contact opening. Embodiments can achieve higher yield by preventing contact to metal gate leakage because of the more robust spacers and etch stop layer.

An embodiment is a method comprising diffusing carbon through a surface of a substrate, implanting carbon through the surface of the substrate, and annealing the substrate after the diffusing the carbon and implanting the carbon through the surface of the substrate. The substrate comprises a first gate, a gate spacer, an etch stop layer, and an inter-layer dielectric. The first gate is over a semiconductor substrate. The gate spacer is along a sidewall of the first gate. The etch stop layer is on a surface of the gate spacer and over a surface of the semiconductor substrate. The inter-layer dielectric is over the etch stop layer. The surface of the substrate comprises a surface of the inter-layer dielectric.

Another embodiment is a method comprising forming a first gradient of carbon in a direction from a surface of a substrate to a first depth in the substrate below the surface of the substrate; forming a second gradient of carbon in a direction from the surface of the substrate to a second depth in the

substrate below the first depth; and after the forming the first gradient of carbon and the forming the second gradient of carbon, annealing the substrate. The forming the first gradient of carbon includes exposing the surface of the substrate to a carbon-containing plasma. The forming the second gradient of carbon includes implanting carbon through the surface of the substrate. The substrate comprises a gate spacer, an etch stop layer, and an inter-layer dielectric. The gate spacer is along a sidewall of a first gate, and the gate spacer is over a semiconductor substrate. The etch stop layer is along a surface of the gate spacer and over the semiconductor substrate. The inter-layer dielectric is over the etch stop layer.

A further embodiment is a structure comprising a gate over a semiconductor substrate, a gate spacer along a sidewall of the gate, an etch stop layer over the gate spacer and over the semiconductor substrate, and an inter-layer dielectric over the etch stop layer. A first portion of the gate spacer is distally located from the semiconductor substrate, and a second portion of the gate spacer is proximally located to the semiconductor substrate. The first portion has a higher concentration of carbon than the second portion. A third portion of the etch stop layer is distally located from the semiconductor substrate, and a fourth portion of the etch stop layer is proximally located to the semiconductor substrate. The third portion has a higher concentration of carbon than the fourth portion.

Although the present embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method comprising:

diffusing carbon through a planar surface of a substrate, the substrate comprising:

a first gate over a semiconductor substrate,

a gate spacer along a sidewall of the first gate,

an etch stop layer on a surface of the gate spacer and over a surface of the semiconductor substrate, and

an inter-layer dielectric over the etch stop layer, wherein the planar surface of the substrate includes a surface of the etch stop layer and a surface of the inter-layer dielectric; and

implanting carbon through the planar surface of the substrate; and

annealing the substrate after the diffusing carbon and the implanting carbon through the planar surface of the substrate.

2. The method of claim **1**, wherein the diffusing carbon through the planar surface of the substrate includes exposing the planar surface of the substrate to a carbon-containing plasma.

3. The method of claim **1**, wherein the implanting carbon through the planar surface of the substrate implants carbon into a portion of the gate spacer and a portion of the etch stop layer along the surface of the gate spacer.

4. The method of claim **1**, wherein the implanting carbon is performed at an angle normal to the planar surface of the substrate.

5. The method of claim **1**, wherein the implanting carbon is performed with a first implantation at a first angle that is not normal to the planar surface of the substrate and with a second implantation at a second angle complementary to the first angle.

6. The method of claim **1** further comprising removing the first gate after the annealing the substrate, and forming a second gate in a region where the first gate was removed.

7. The method of claim **1** further comprising etching a contact opening through the inter-layer dielectric and the etch stop layer to source/drain regions formed in the semiconductor substrate.

8. The method of claim **1**, wherein before the diffusing carbon and the implanting carbon, the gate spacer and the etch stop layer each comprise silicon nitride.

9. A method comprising:

forming a first gradient of carbon in a direction from a surface of a substrate to a first depth in the substrate below the surface of the substrate, the forming the first gradient of carbon including exposing the surface of the substrate to a carbon-containing plasma, the substrate comprising:

a gate spacer along a sidewall of a first gate, the gate spacer being over a semiconductor substrate,

an etch stop layer along a surface of the gate spacer and over the semiconductor substrate, and

an inter-layer dielectric over the etch stop layer;

forming a second gradient of carbon in a direction from the surface of the substrate to a second depth in the substrate below the first depth, the forming the second gradient of carbon including implanting carbon through the surface of the substrate; and

after the forming the first gradient of carbon and the forming the second gradient of carbon, annealing the substrate.

10. The method of claim **9**, wherein the first gradient of carbon includes a concentration of carbon that decreases in the direction from the surface of the substrate to the first depth, and wherein the second gradient of carbon includes a concentration of carbon that increases and subsequently decreases in the direction from the surface of the substrate to the second depth.

11. The method of claim **9**, wherein the exposing the surface of the substrate to a carbon-containing plasma forms the first gradient of carbon by diffusing carbon.

12. The method of claim **9**, wherein the implanting carbon through the surface of the substrate is performed at an angle normal to the surface of the substrate.

13. The method of claim **9**, wherein the implanting carbon through the surface of the substrate comprises a first implantation at a first implantation angle and a second implantation at a second implantation angle complementary to the first implantation angle.

14. The method of claim **9** further comprising removing the first gate after the annealing the substrate, and forming a second gate in a region where the first gate was removed.

15. The method of claim **9** further comprising etching a contact opening through the inter-layer dielectric and the etch stop layer to the semiconductor substrate.

16. A method comprising:

densifying a first portion of a substrate, the first portion of the substrate comprising:

a first portion of an etch stop layer on a gate structure, the gate structure being over a semiconductor substrate, and

a first portion of an inter-layer dielectric over the etch stop layer,

wherein the densifying includes introducing carbon into the first portion of the etch stop layer on the gate structure and the first portion of the inter-layer dielectric over the etch stop layer; and

after the densifying, forming a contact through the inter-layer dielectric and the etch stop layer to the semiconductor substrate.

17. The method of claim **16**, wherein the densifying comprises:

diffusing carbon into the first portion of the etch stop layer on the gate structure and the first portion of the inter-layer dielectric over the etch stop layer;

implanting carbon into the first portion of the etch stop layer on the gate structure and the first portion of the inter-layer dielectric over the etch stop layer; and

after the diffusing and the implanting, annealing the substrate.

18. The method of claim **16**, wherein the densifying comprises:

exposing the first portion of the etch stop layer on the gate structure and the first portion of the inter-layer dielectric over the etch stop layer to a carbon-containing plasma;

implanting carbon into the first portion of the etch stop layer on the gate structure and the first portion of the inter-layer dielectric over the etch stop layer; and

after the exposing and the implanting, annealing the substrate.

19. The method of claim **16**, wherein after the densifying, a second portion of the substrate has a lower concentration of carbon than the first portion of the substrate, the second portion of the substrate comprising:

a second portion of the etch stop layer; and

a second portion of the inter-layer dielectric.

20. The method of claim **16**, wherein a concentration of carbon in the first portion of the substrate after the densifying is substantially uniform.

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